

Docket No.: GR 97 P 6457

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JÖRG BERTHOLD ET AL.

Filed : Concurrently herewith

Title : INTEGRATED ELECTRICAL CIRCUIT AND METHOD FOR
FABRICATING IT

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Leurs
12/15/00

JC812 U.S. PTO
09/595860



INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications
are submitted herewith:

U.S. Patent No. 5,025,741 (Suwanai et al.), dated June 25, 1991;

U.S. Patent No. 5,723,382 (Sandhu et al.), dated March 3, 1998;

German Patent No. 195 43 540 C1 (Lauterbach et al.), dated November 21, 1996,
pertains to a vertical integrated semiconductor component with two connected
substrates and a method for producing the same;

Published European Patent Application No. 0 751 566 A2 (Cabral et al.), dated
January 2, 1997;

Published European Patent Application No. 0 261 846 A1 (Hoshino), dated March
30, 1988;

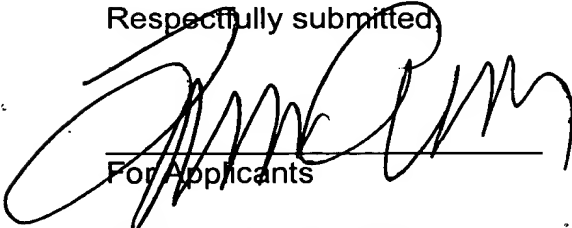
"Barrier Metal Free Copper Damascene Interconnection Technology Using
Atmospheric Copper Reflow and Nitrogen Doping in SiOF Film", K. Mikagi et al.,
IEEE, 1996, pp. 365-368;

"Evaluation of a Copper Metallization Process and the Electrical Characteristics of Copper-Interconnected Quarter-Micron CMOS", Nobuyoshi Awaya et al., IEEE Transactions on Electron Devices, Vol. 43, No. 8, August 1996, pp. 1206-1212 and

"Integration of copper multilevel interconnects with oxide and polymer interlevel dielectrics", Ronald J. Gutmann et al., Thin Solid Films 270, 1995, pp. 472-479.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted



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For Applicants

Date: June 16, 2000

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